

We claim:

- 1 1. A method of cooling a semiconductor chip, comprising:
2 providing a number of electrical devices on a semiconductor layer of the
3 semiconductor chip;
4 integrally forming a substantially planar heat conducting layer with the
5 semiconductor layer, wherein the heat conducting layer is compatible with
6 semiconductor processing techniques, the heat conducting layer being adjacent to
7 the number of electrical devices, the heat conducting layer having a higher thermal
8 conductivity than the semiconductor layer;
9 conducting heat generated by the number of electrical devices into the heat
10 conducting layer; and
11 transmitting the heat generated by the number of electrical devices through
12 the heat conducting layer from a first region having a first temperature to a second
13 region having a second temperature that is lower than the first region.
- 1 2. The method of claim 1, wherein providing a number of electrical devices
2 includes providing a number of transistors.
- 1 3. The method of claim 1, wherein coupling a heat conducting layer to the
2 semiconductor layer comprises coupling a carbon containing layer to the
3 semiconductor layer.
- 1 4. The method of claim 3 wherein coupling a carbon containing layer to the
2 semiconductor layer comprises coupling a diamond containing layer to the
3 semiconductor layer.
- 1 5. The method of claim 1, further comprising transmitting heat from the heat
2 conducting layer to a location remote from the semiconductor processor chip.

1 6. A method of cooling a semiconductor chip formed from a semiconducting
2 material, comprising:
3 integrally coupling a substantially planar heat conducting layer to the
4 semiconductor chip, wherein the heat conducting layer is compatible with
5 semiconductor processing techniques, the heat conducting layer having a higher
6 thermal conductivity than the semiconducting material;
7 conducting heat from the semiconductor chip into the heat conducting layer;
8 and
9 transmitting the heat through the heat conducting layer from a first region
10 having a first temperature to a second region having a second temperature that is
11 lower than the first temperature.

1 7. The method of claim 6, wherein coupling a substantially planar heat
2 conducting layer to the semiconductor chip includes coupling a carbon containing
3 layer to the semiconductor chip.

1 8. The method of claim 7, wherein coupling a carbon containing layer to the
2 semiconductor chip includes coupling a diamond containing layer to the
3 semiconductor chip.

1 9. The method of claim 6, further comprising transmitting heat from the heat
2 conducting layer to a location remote from the semiconductor chip.

1 10. A method of cooling a semiconductor chip, comprising:
2 integrally forming a diamond containing layer adjacent to a number of
3 electrical devices on a semiconductor layer;
4 conducting heat generated by at least a portion of the number of electrical
5 devices in a first area into the heat conducting layer; and
6 spreading the heat generated by the electrical devices in the first area
7 through the heat conducting layer to a larger second area wherein heat per unit area
8 is reduced.

1 11. The method of claim 10, wherein integrally forming a diamond containing
2 layer adjacent to a number of electrical devices includes integrally forming a
3 diamond containing layer adjacent to a number of transistors.

1 12. The method of claim 10, further comprising transmitting heat from the
2 diamond containing layer to a location remote from the semiconductor processor
3 chip.

1 13. The method of claim 10, wherein integrally forming a diamond containing
2 layer adjacent to a number of electrical devices includes integrally forming a
3 diamond containing layer on an active side of the semiconductor processor chip.

1 14. The method of claim 10, wherein integrally forming a diamond containing
2 layer adjacent to a number of electrical devices includes integrally forming a
3 diamond containing layer on a back side of the semiconductor processor chip.

1 15. The method of claim 10, wherein integrally forming a diamond containing
2 layer adjacent to a number of electrical devices includes integrally forming a
3 diamond containing layer between an active side and a backside of the
4 semiconductor processor chip.

1 16. A method of manufacturing a semiconductor chip, comprising:
2 fabricating a semiconductor layer;
3 forming a number of electrical devices on the semiconductor layer;
4 electrically connecting the number of electrical devices; and
5 integrally forming a substantially planar heat conducting layer operatively
6 connected to the semiconductor layer, wherein the heat conducting layer is
7 compatible with semiconductor processing techniques, the heat conducting layer
8 being adjacent to the number of electrical devices, the heat conducting layer having
9 a higher thermal conductivity than the semiconductor layer.

1 17. The method of claim 16, wherein fabricating a semiconductor layer includes
2 fabricating a silicon substrate.

1 18. The method of claim 16, wherein forming a substantially planar heat
2 conducting layer includes forming a carbon containing layer.

1 19. The method of claim 18, wherein forming a carbon containing layer includes
2 forming a diamond containing layer.

1 20. The method of claim 19, wherein forming a diamond containing layer
2 includes chemical vapor deposition (CVD) depositing a diamond layer.

1 21. A method of manufacturing a semiconductor chip, comprising:
2 forming a number of transistors on a semiconductor layer;
3 electrically connecting the number of transistors; and
4 integrally forming a substantially planar diamond containing layer
5 operatively connected to the semiconductor layer, and adjacent to the number of
6 transistors.

1 22. The method of claim 21, wherein forming a number of transistors on a
2 semiconductor layer includes forming a number of transistors on a silicon substrate.

1 23. The method of claim 21, wherein integrally forming a substantially planar
2 diamond containing layer operatively connected to the semiconductor layer, and
3 adjacent to the number of transistors includes integrally forming a substantially
4 planar diamond containing layer on an active side of the semiconductor chip.

1 24. The method of claim 21, wherein integrally forming a substantially planar
2 diamond containing layer operatively connected to the semiconductor layer, and

3 adjacent to the number of transistors includes integrally forming a substantially
4 planar diamond containing layer on a back side of the semiconductor chip.

1 25. The method of claim 21, wherein integrally forming a substantially planar
2 diamond containing layer operatively connected to the semiconductor layer, and
3 adjacent to the number of transistors includes integrally forming a substantially
4 planar diamond containing layer between an active side and a back side of the
5 semiconductor chip.

1 26. A method of forming an electronic system, comprising:
2 forming a processor chip, including:
3 forming a number of transistors on a semiconductor layer;
4 electrically connecting the number of transistors;
5 integrally forming a substantially planar diamond containing layer
6 operatively connected to the semiconductor layer, and adjacent to the number of
7 transistors; and
8 coupling the processor chip to a random access memory.

1 27. The method of claim 26, wherein forming a substantially planar diamond
2 containing layer includes chemical vapor deposition (CVD) depositing a diamond
3 layer.